UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/986,577	11/09/2001	Takashi Hiroi	501.40830VX1	5835

20457 7590 12/13/2005

ANTONELLI, TERRY, STOUT & KRAUS, LLP
1300 NORTH SEVENTEENTH STREET
SUITE 1800
ARLINGTON, VA 22209-3873

EXAMINER	
STREGE, JOHN B	
ART UNIT	**PAPER NUMBER**
2625	

DATE MAILED: 12/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/986,577	HIROI ET AL.	
	Examiner	Art Unit	
	John B. Strege	2625	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *28-30 and 32-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 May 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/12/05 has been entered.

Terminal Disclaimer

The terminal disclaimer filed on 9/13/05 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of any patent granted on case 09/986,299 has been reviewed and is accepted. The terminal disclaimer has been recorded.

Response to Amendment

The amendment received on 9/13/05 has been entered in full.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 28-30, and 32-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gallarda et al. USPN 6,539,106 (hereinafter "Gallarda").

Regarding claim 29, Gallarda discloses a pattern inspection apparatus comprising: image detecting means for attaining a digital image of an object substrate on which a pattern is formed through microscopic observation thereof (col. 3 lines 23-29, and col. 16 lines 27-34 disclose that the test image can be from a scanning-electron-microscope); a display having a screen on which the digital image of the object substrate is displayable (figure 3 numeral 345 discloses a map of the substrate which is a digital image since it is derived from a digital image); defect detecting means for detecting defects of the pattern formed on said object substrate by comparing the digital image attained by the image detecting means with a reference image while masking a pre-registered region or a pattern matching with a pre-registered pattern (col. 3 lines 19-55 disclose preparing a reference image and a test image, extracting features from the reference image and extracting features from the test image, and comparing features of the reference image and of the test image to identify defects, wherein the extracting features from an image can comprise matching a feature template in the image and identifying features in the image that match the feature-template [masking]); and output means for outputting data regarding the defects detected by the defect detecting means including digital images of said defects detected by masking and the positional distribution data thereof in a map form (figure 3 numeral 345 discloses a display for outputting a defect map, defect location, size, type, etc.). Gallarda discloses using a guided user interface (GUI, figure 3, col. 6 lines 6-9) to carry out the inspection and

further that intermediate images and results such as a map of defects and statistics about defect location, size, type, etc. are shown on the display (col. 6 lines 26-35). The map of the defects comes from the actual images of the patterned substrates (as seen in figure 3), thus as a map of the defects is shown this map constitutes actual image data of each of the detected defects. Thus each of the defects on the map can be read as an actual image of a defect among the defects detected. Gallarda does not explicitly disclose that the preregistered region or pattern is inputted and displayed on a display screen, however Gallarda does disclose the template region (the template is a preregistered region) which is a region found within the semiconductor wafer. As the map of the defects is displayed then the feature regions of the template must also be displayed on the map, thus reading on the limitation of displaying the pre-registered region on the display screen.

Regarding claim 28, Gallarda discloses an image detecting part for detecting a digital image of an object substrate (col. 3 lines 23-29, and col. 16 lines 27-34 disclose that the test image is digital); a display having a screen on which the digital image of the object substrate is displayable (figure 3 numeral 345 discloses a map of the substrate which is a digital image since it is derived from a digital image) a memory part for storing coordinate data, pattern data or feature quantity data of the non-inspection region to be masked in the object substrate on which a pattern is formed (a template is disclosed which is a mask [col. 3 lines 53-55], the template image is stored in memory [col. 6 lines 6-15]); a defect judging part in which the digital image detected by the image detecting part is examined in a state that a region matching with a condition

stored in the memory part is masked and detecting a defect (col. 3 lines 19-63); and a display having a screen on which a digital image of the detected defect is displayed together with positional information of the detected defect in a map form (figure 3 numeral 345). Gallarda discloses using a guided user interface (GUI, figure 3, col. 6 lines 6-9) to carry out the inspection and further that intermediate images and results such as a map of defects and statistics about defect location, size, type, etc. are shown on the display (col. 6 lines 26-35). The map of the defects comes from the actual images of the patterned substrates (as seen in figure 3), thus as a map of the defects is shown this map constitutes actual image data of each of the detected defects. Thus each of the defects on the map can be read as an actual image of a defect among the defects detected. Gallarda does not explicitly disclose that the preregistered region or pattern is inputted and displayed on a display screen, however Gallarda does disclose the template region (the template is a preregistered region) which is a region found within the semiconductor wafer. As the map of the defects is displayed then the feature regions of the template must also be displayed on the map, thus reading on the limitation of displaying the pre-registered region on the display screen.

Regarding claim 30, Gallarda discloses that the reference image and test image can be obtained using a scanning-electron-microscope (col. 16 line10-34) and a feature template can be used to aid in the feature extraction for a particular type of image can be used to extract the features (col. 17 lines 45-59), thus it is inherent that if the feature template is to be used with a microscopic reference and test images then it must be set up using a microscopic image.

Claims 32 and 34 are similar to claim 29 with the additional limitation of a defect extracting means. Gallarda discloses a defect extraction means (col. 3 lines 19-29). The rest of the limitations have already been addressed above.

Regarding claims 33 and 35, Gallarda discloses that the reference image and test image can be obtained using a scanning-electron-microscope (col. 16 line10-34) and a feature template can be used to aid in the feature extraction for a particular type of image can be used to extract the features (col. 17 lines 45-59), thus it is inherent that if the feature template is to be used with a microscopic reference and test images then it must be set up using a microscopic image.

Regarding claim 36, Gallarda discloses displaying defect data such as a defect map, defect location, defect size, defect type, etc (figure 3 numeral 345).

Claim 37 is similar to claim 34 with the additional limitations of defect classifying means for classifying the extracted defects by using the feature quantiy data; and output means for outputting class data of each of the defects classified by the defect classifying means together with the feature quantity data thereof. Gallarda discloses displaying the type of the defect (figure 3 numeral 345), thus the defect must be classified. The type of defect is output with the defect map, position, size, etc.

Regarding claim 38, Gallarda discloses displaying the type of defect (classification) on the display screen (figure 3 numeral 345).

Response to Arguments

Applicant's arguments filed 9/13/05 have been fully considered but they are not persuasive. Specifically the Applicants argue that Gallarda does not disclose an actual

image of the defect. As the defect map is derived from an actual test image of the patterned substrate (see discussion above), it constitutes an actual image.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B. Strege whose telephone number is (571) 272-7457. The examiner can normally be reached on Monday-Friday between the hours of 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bhavesh Mehta can be reached on (571) 272-7453. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JS

BHAVESH M. MEHTA
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600